EM78910/910A

8-BIT MICRO-CONTROLLER

Version 1.0

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Version History

Specification Revision History		
Version	**Content**	**Release Date**
EM78910/910A		
1.0	Initial version	2001/1/12

I.General Description

The EM78910/910A is an 8-bit CID (Call Identification) RISC type microprocessor with low power, high speed CMOS technology. This integrated single chip has on_chip watchdog (WDT), RAM, ROM, programmable real time clock/counter, internal interrupt, power down mode, FSK decoder, Call waiting decoder, SDT (Stuttered dial tone) decoder, DTMF generator, MEI (Multiple Extension Internetworking) function, RTF (Request To Flash) function and tri-state I/O. The EM78910/910A provides a single chip solution to design a CID of calling message_display.

II. Feature

CPU

- Operating voltage range : 2.5V～5.5V
- 16K × 13 Read Only Memory
- 1.1K× 8 on chip RAM
- Up to 28 bi-directional tri-state I/O ports
- 8 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- Two sets of 8 bit counters can be interrupt sources
- Selective signal sources and trigger edges , and with overflow interrupt
- Programmable free running on chip watchdog timer
- 99.9% single instruction cycle commands
- Four modes (Main clock 3.579MHz or 1.79MHz)

  Set code option bit0(MCLK) : 0/1 ➔ 3.579MHz/1.79MHz

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Idle mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- Ring on voltage detector
- Universal Low battery detector
- Input port wake up function
- 9 interrupt source , 4 external , 5 internal
- Port key scan function
- Clock frequency 32.768KHz
- Eight R-option pins

CID

- Bell 202 , V.23 FSK demodulator
- DTMF generator
- Ring detector on chip

CALL WAITING

- Compatible with Bellcore special report SR-TSV-002476
- Call-Waiting (2130Hz plus 2750Hz) alert signal detection
- Good talkdown and talkoff performance
- Sensitivity compensated by adjusting input OP gain

SDT

- Stuttered Dial Tone (350Hz plus 440Hz) signal detection

MEI/RTF

- Compatible with TIA/EIA-777(TIA SP-4078)
- MEI(Multiplex Extension Internetworking) and RTF(Request To Flash) functions

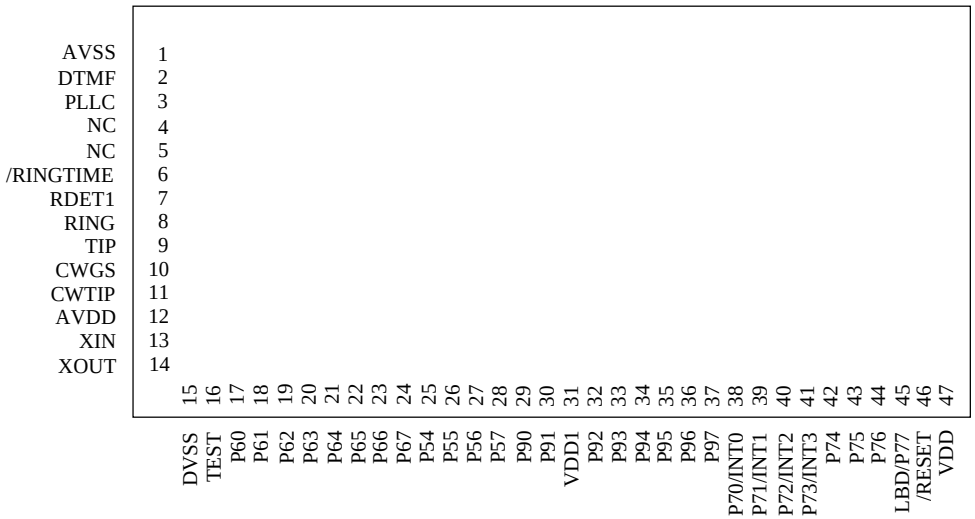
PACKAGE

- **45-pin die form without MEI/RTF** (**EM78910**AH, POVD disable)(**EM78910**BH, POVD enable)
- **47-pin die form with MEI/RTF** (**EM78910A**AH, POVD disable)(**EM78910A**BH, POVD enable)

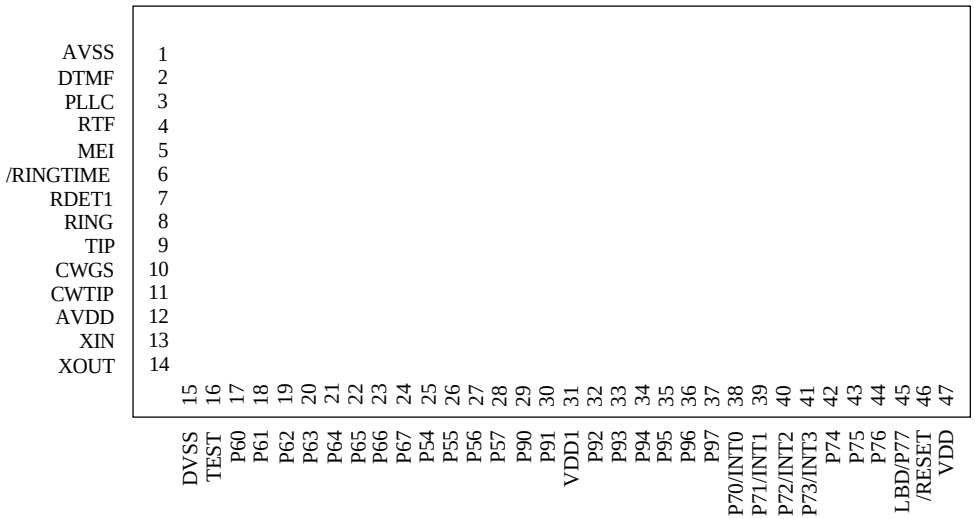
III. Application

1. Adjunct units
2. Answering machines
3. Feature phones

IV. Pin Configuration



45-pin die **EM78910**AH, **EM78910**BH



47-pin die **EM78910A**AH, **EM78910A**BH

Fig.1 Pin Assignment

V. Functional Block Diagram

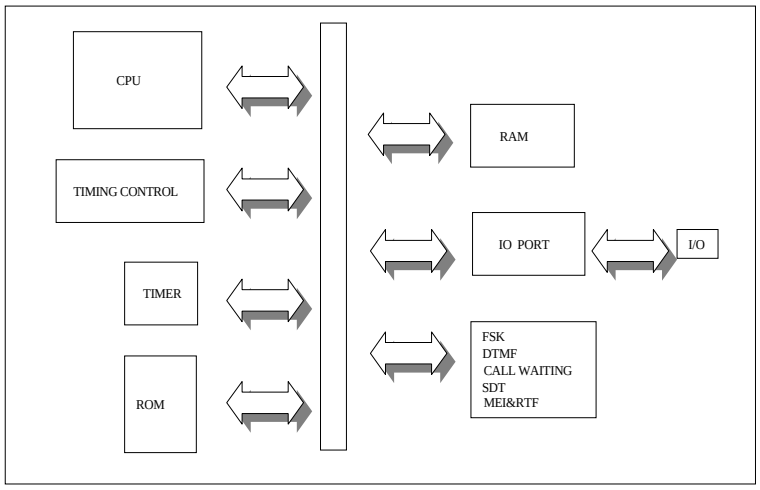


Fig.2 Block diagram1

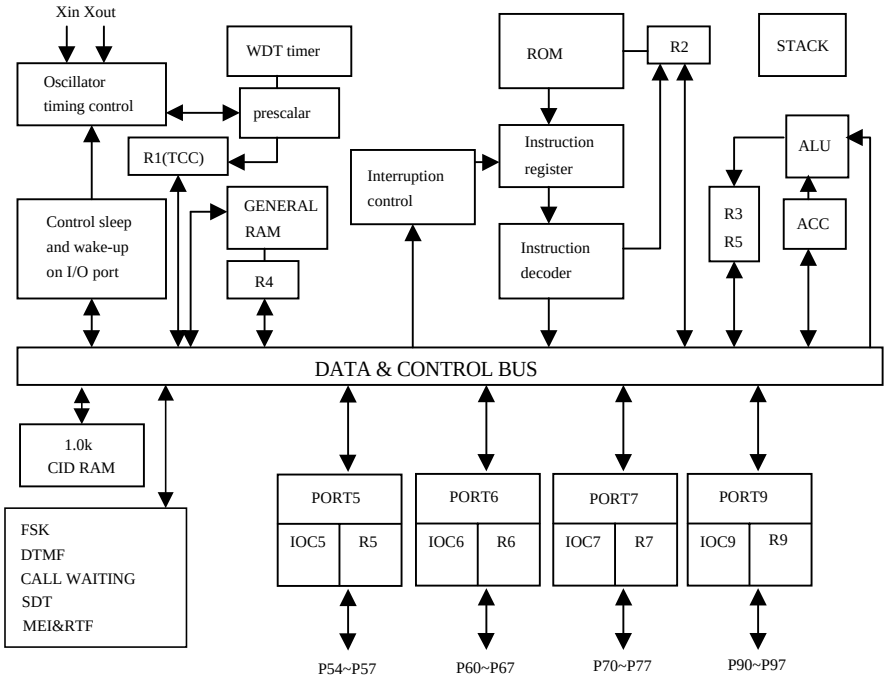


Fig.3 Block diagram2

VI. Pin Descriptions

PIN	I/O	DESCRIPTION
VDD, VDD1 AVDD	POWER	Digital power Analog power
VSS AVSS	POWER	Digital ground Analog ground
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with AVSS
RTF	I	Request to flash input. Detect line DC voltage changed
MEI	I	Multiple extension internetworking input. 1.2 DC voltage detection can be used as on-hook/off-hook detection.
TIP	I	It should be connected with TIP side of twisted pair lines for FSK.
RING	I	It should be connected with RING side of twisted pair lines for FSK.
CWTIP	I	It should be connected with TIP side of twisted pair lines for CW.
CWGS	I	The input OP output pin for gain adjustment of CW.
RDET1	I	It detect the energy on the twisted pair lines. This pin is coupled to the twisted pair lines through an attenuating network for ring signal detect.
/RINGTIME	I	Determine if the incoming ring is valid. A RC network may be connected to the pin.
INT0 INT1 INT2 INT3 	PORT7(0) PORT7(1) PORT7(2) PORT7(3) PORT7(4:7)	PORT7(0)~PORT7(3) signal can be interrupt signals. INT2 and INT3 has the same interrupt flag. IO port
P5.4 ~P5.7	PORT5	PORT 5 can be INPUT or OUTPUT port each bit.
P6.0 ~P6.7	PORT6	PORT 6 can be INPUT or OUTPUT port each bit.
P7.0 ~P7.7	PORT7	PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Key scan function.
P9.0 ~P9.7	PORT9	PORT 9 can be INPUT or OUTPUT port each bit. And can be set to wake up watchdog timer.
TEST	I	Test pin into test mode , normal low
DTMF	O	DTMF tone output
/RESET	I	reset

VII. Functional Descriptions

VII.1 Operational Registers

1. R0 (Indirect Addressing Register)
   * R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).
2. R1 (TCC)
   * Increased by an external signal edge applied to TCC, or by the instruction cycle clock.
   * Written and read by the program as any other register.
3. R2 (Program Counter)
   * The structure is depicted in Fig.4.
   * Generates 16K × 13 on-chip ROM addresses to the relative programming instruction codes.
   * "JMP" instruction allows the direct loading of the low 10 program counter bits.
   * "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.
   * "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
   * "MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
   * "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
   * "TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the content of bit PS0~PS2 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

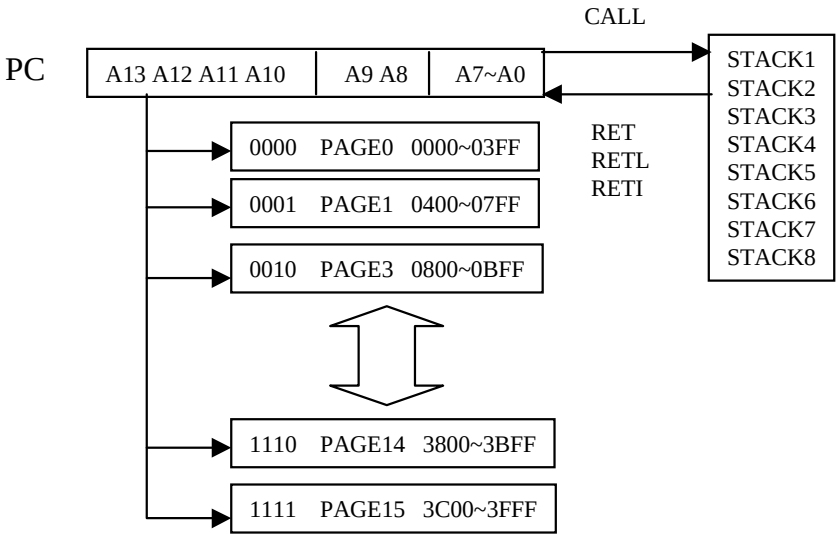


Fig.4 Program counter organization

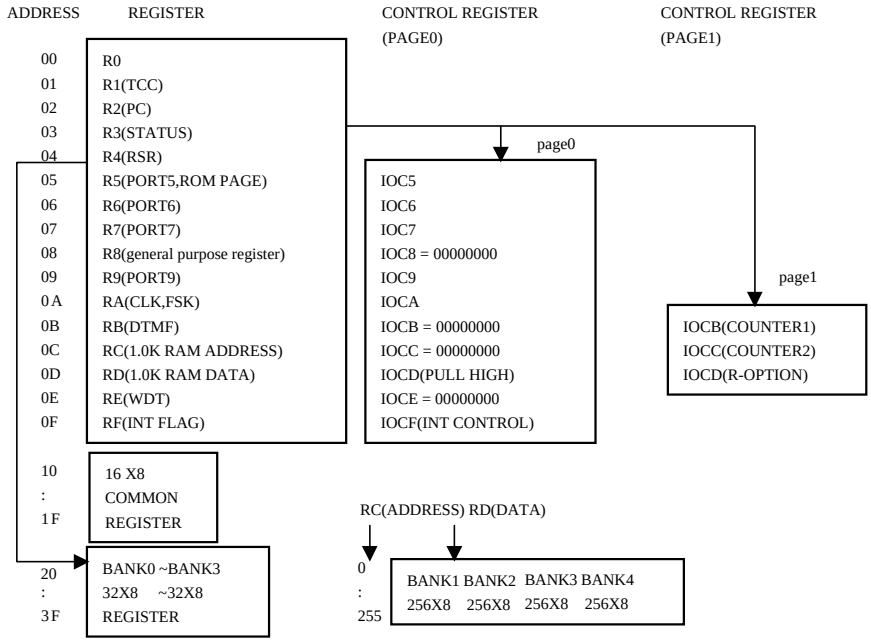


Fig.5 Data memory configuration

4. R3 (CW and SDT output, CPU power control, Register page selection, Status flags)

7	6	5	4	3	2	1	0
CAS	PAGE	/SDT	T	P	Z	DC	C

* Bit 0 (C) : Carry flag
* Bit 1 (DC) : Auxiliary carry flag
* Bit 2 (Z) : Zero flag
* Bit 3 (P) : Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
* Bit 4 (T) : Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode	0	1	
/RESET wake up from sleep	1	0	
power up	1	1	
Low pulse on /RESET	x	X	X : don't care

* Bit 5 (/SDT) : (Read Only) Stuttered dial tone signal detection output, 0/1 => SDT signal valid/SDT signal invalid
* Bit 6 (PAGE) : Change IOCB ~ IOCE to another page, 0/1 ➔ PAGE0/PAGE1
* Bit 7 (CAS) : (Read Only) Call waiting signal detection output, 0/1 ➔ CW signal valid/signal invalid

5. R4 (RAM address selection)

* Bits 0 ~ 5 are used to select up to 64 registers in the indirect addressing mode.
* Bits 6 ~ 7 determine which bank is activated among the 4 banks.
* See the configuration of the data memory in Fig.5.

6. R5 (PORT5(7:4) I/O registers, Program page selection)

7	6	5	4	3	2	1	0
R57	R56	R55	R54	PS3	PS2	PS1	PS0

* Bit 3~0 (PS3~PS0) : Program page selection bits

Program page select bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
0	1	0	0	Page 4
0	1	0	1	Page 5
0	1	1	0	Page 6
0	1	1	1	Page 7
1	0	0	0	Page 8
1	0	0	1	Page 9
1	0	1	0	Page 10
1	0	1	1	Page 11
1	1	0	0	Page 12
1	1	0	1	Page 13
1	1	1	0	Page 14
1	1	1	1	Page 15

User can use PAGE instruction to change page and maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. The program page is maintained by EMC's complier. It will change user's program by inserting instructions within program.

* Bit 7~4 (R57 ~ R54) : 4-bit I/O register for PORT57~PORT53 I/O

7. R6,R7 and R9 (I/O registers for PORT6, PORT7 and PORT9)

* R6, R7 and R9 are four 8-bit I/O registers for PORT6, PORT7 and PORT9.

8. R8 (General-purpose)

* R8 is a general-purpose register.

9. RA (CPU mode selection, Low battery detection, FSK power and output status, Ring detection output)

7	6	5	4	3	2	1	0
IDLE	ENPLL	/LPD	/LOW_BAT	/FSKPWR	DATA	/CD	/RD

* Bit 0 (/RD) : (Read Only) Ring signal detection output, 0/1 ➔ Ring signal valid/Ring signal invalid
* Bit 1 (/CD) : (Read Only) FSK carrier signal detection output, 0/1 ➔ Carrier signal valid/Carrier signal invalid
* Bit 2 (DATA) : (Read Only)(FSK demodulator output signal)
  Fsk data transmitted in a baud rate 1200 Hz.
* Bit 3 (/FSKPWR) : Power up/down FSK block, 1/0 ➔ power up FSK block/power down FSK block
  When FSK is powered on, PLL is also enabled regardless of RA bit 6 (ENPLL). When FSK is powered off, PLL status is depended on RA bit 6 (ENPLL) setting.

The relation between Bit 0 to Bit 3 is shown in Fig.6.

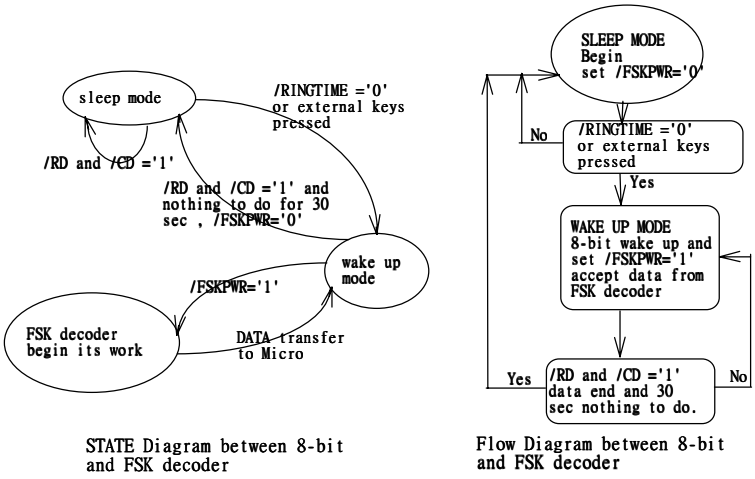


Fig.6 The relation between Bit0 to Bit3.

* Bit 4 (/LOW-BAT) : (Read Only) Low battery detection output, 0/1 ➔ Battery voltage is low/Normal.
Low battery detection level is set by external resisters R1 and R2. The detection level VbL = 0.87V*(1+ R1/R2). If Vbattery is under VbL, then send a '0' signal to /LOW_BAT bit; othwise a '1' signal to this bit. Select pin P77/LBD as LBD by setting IOCE PAGE0 bit1 to '0'. LBD pin is used as low battery detection input.
* Bit 5 (/LPD) : Power control of low battery detector, 0/1 ➔ Power on low battery detector/power off low battery detector
The relation between /LPD, /POVD(see code option) and /LOW_BAT can see Fig7

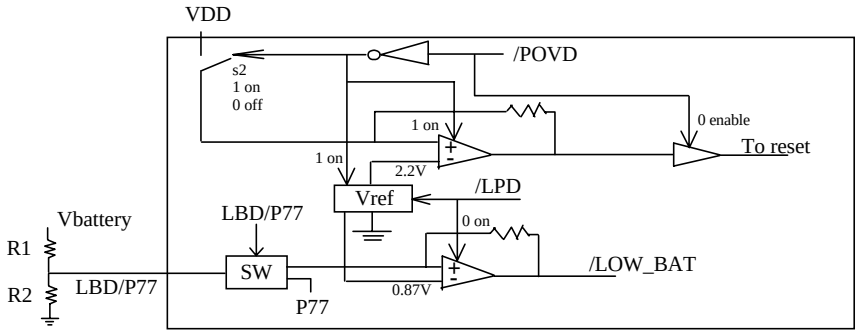


Fig.7 Universal low battery detector with /LPD, /POVD and /LOW_BAT

* Bit 6 (ENPLL) : PLL enable/disable control, 1/0 ➔ enable/disable
When ENPLL is enabled, CPU is in the normal mode
The relation between 32.768kHz and 3.579MHz can see Fig8.

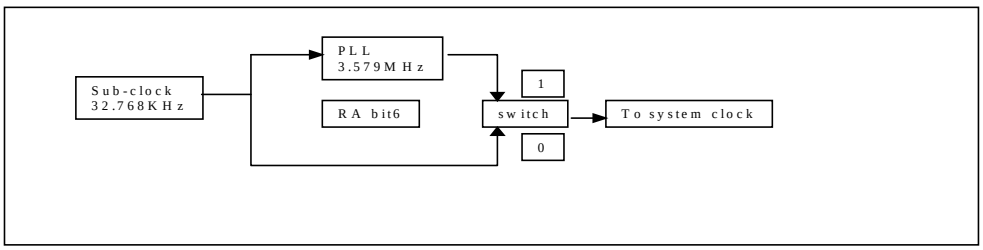


Fig.8 The relation between 32.768kHz and 3.579MHz .

* Bit 7 (IDLE) : CPU power saving mode selection bit, 0/1 ➔ select sleep mode/select IDLE mode.
This bit will decide which CPU power saving mode is selected for SLEP instruction.
These two modes can be waken up by TCC clock or WatchDog or PORT9 and run from "SLEP" next instruction.

Wakeup signal	SLEEP mode	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out	X	Wakeup + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wakeup + Next instruction	RESET	RESET
PORT9 /RINGTIME pin	RESET	Wakeup + Next instruction	X	X
PORT70~73	X	Wakeup + Interrupt + Next instruction	Interrupt	Interrupt

P70 ~ P73 's wakeup functions are controlled by IOCF(1,2,3) and ENI instruction.
P70 's wakeup signal is a rising or falling signal defined by CONT REGISTER bit7.
/RINGTIME pin, Port9, Port71, Port72 and Port73 's wakeup signal is a falling edge signal.

10. RB (DTMF row-freq. and column-freq tone selections)(write/write)

7	6	5	4	3	2	1	0
C3	C2	C1	C0	R3	R2	R1	R0

* Bit 3~0 (R3~R0) : DTMF row-frequency tone selection bits.
* Bit 7~4 (C3~C0) : DTMF column-frequency tone selection bits.
When bit 7~0 of RB are all "1", DTMF generator is power off.

	Bit 7~4 (column freq.)			
Bit 3~0 (row freq.)	1110 (1203.0Hz)	1101 (1331.8Hz)	1011 (1472Hz)	0111 (1645.2Hz)
1110 (699.2Hz)	1	2	3	A
1101 (771.6Hz)	4	5	6	B
1011 (854.0Hz)	7	8	9	C
0111 (940.1Hz)	*	0	#	D

11. RC (Caller ID RAM address selection)(read/write)

7	6	5	4	3	2	1	0
CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0

* Bit 7~0 (CIDA7~CIDA0) : Caller ID RAM address selection bits
User can select Caller ID RAM address up to 256.

12. RD (Caller ID RAM data)(read/write)
* Bit 8 ~ Bit 0 are Caller ID RAM data transfer register.
User can see IOCA register how to select CID RAM banks.

13. RE (CW power control, WDT control, Wakeup control)(read/write)

7	6	5	4	3	2	1	0
CWPWR	/WDTE	/WUP9H	/WUP9L	/WURING	0	0	0

* Bit 0~2 = 0 : unused
* Bit 3 (/WURING) : Ring wakeup control, 1/0 ➔ enable/disable
It is used to enable the wakeup function of /RINGTIME input pin.
* Bit 4 (/WUP9L) : PORT9's low nibble wakeup control, 1/0 ➔ enable/disable
It is used to enable the wakeup function of low nibble for PORT9.

* Bit 5 (/WUP9H) : PORT9's high nibble wakeup control, 1/0 ➔ enable/disable
  It is used to enable the wakeup function of high nibble for PORT9.
* Bit 6 (/WDTE) : Watchdog timer control, 1/0 ➔ enable/disable
  It is used to enable/disable Watchdog timer.
  The relation between Bit3 to Bit6 can see the diagram 9.
* Bit 7(CWPWR) : Power control of Call waiting circuit, 1/0 ➔ power up circuit /power down circuit
  When Call waiting circuit is powered on, PLL is also enabled regardless of RA bit 6(ENPLL). When Call waiting circuit is powered off, PLL status is depended on RA bit 6 (ENPLL) setting.

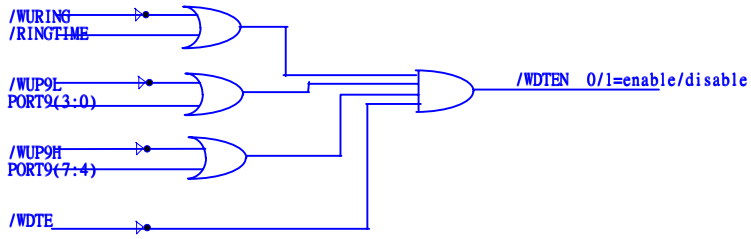


Fig.9 Wake up function and control signal

14. RF (Interrupt status register)

7	6	5	4	3	2	1	0
INT3	FSK/CW	C8_2	C8_1	INT2	INT1	INT0	TCIF

* Bit 0 (TCIF) : TCC timer overflow interrupt flag. Set when TCC timer overflows.
* Bit 1 (INT0) : External INT0 pin interrupt flag
* Bit 2 (INT1) : External INT1 pin interrupt flag
* Bit 3 (INT2) : External INT2 pin interrupt flag
* Bit 4 (C8_1) : Internal 8 bit counter interrupt flag
* Bit 5 (C8_2) : Internal 8 bit counter interrupt flag
* Bit 6 (FSK/CW) : FSK data or Call waiting data interrupt flag
* Bit 7 (INT3) : External INT3 pin interrupt flag.

High to low edge trigger. Refer to the Interrupt subsection.
IOCF is the interrupt mask register. User can read and clear.
"1" means interrupt request, "0" means non-interrupt

15. R10~R3F (General Purpose Register)

* R10~R3F (Banks 0~3) are all general-purpose registers.

VII.2 Special Purpose Registers

1. A (Accumulator)

Internal data transfer, or instruction operand holding
It's not an addressable register.

2. CONT (Control Register : P70 interrupt edge, INT flag, TCC edge, precaler rate selection for TCC or WDT)

7	6	5	4	3	2	1	0
INT_EDGE	INT	TS	TE	PAB	PSR2	PSR1	PSR0

* Bit 2~0 (PSR2~PSR0) : TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

* Bit 3 (PAB) : Prescaler assignment bit, 0/1 ➔ prescaler for TCC/prescaler for WDT
* Bit 4 (TE) : TCC signal edge
  0 ➔ increment from low to high transition on TCC
  1 ➔ increment from high to low transition on TCC
* Bit 4 : unused
* Bit 5 (TS) : TCC signal source, 0/1 ➔ internal instruction cycle clock/16.384kHz
* Bit 6 (INT) : INT enable flag
  0 ➔ interrupt masked by DISI or hardware interrupt
  1 ➔ interrupt enable by ENI/RETI instructions
* Bit 7 (INT_EDGE) : Interrupt edge control of P70, 0/1 ➔ rising edge interrupt/falling interrupt

CONT register is readable and writable.

3. IOC5 (PORT5(7:4) I/O control, MEI and RTF output, RTF power control)

7	6	5	4	3	2	1	0
IOC57	IOC56	IOC55	IOC54	MEIO	RTFO	RTFPWR	0

* Bit 0 = 0 : unused
* Bit 1 (RTFPWR) : Power control of RTF circuit, 1/0 ➔ power on/power off
* Bit 2 (RTFO) : (Read Only) RTF line DC voltage change detect output.
  When line DC voltage is not changed, RTFO is high.
* Bit3 (MEIO) : (Read Only) MEI line high or line in-use detect output
  When input voltage of MEI pin is below 1.2V, MEIO is low; when input voltage of MEI pin is over 1.3V, MEIO is high.
* Bit 4 ~7 (IOC54 ~ IOC57) : PORT5 I/O direction control registers.

"1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.

4. IOC6, IOC7 and IOC9 (I/O port control register for PORT6, PORT7 and PORT9)

IOC6, IOC7 and IOC9 are four I/O direction control registers for PORT6, PORT7 and PORT9.
"1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
User can see IOCB register how to switch to normal I/O port.

5. IOC8 (unused)

IOC8 is unused and always "00000000".

6. IOCA (CALLER ID RAM,IO ,PAGE Control Register)(read/write,initial "00000000")

7	6	5	4	3	2	1	0
0	0	SDTPW/0	0	0	CALL_2	CALL_1	MEIPWR

* Bit 0(MEIPWR) : power control of MEI circuit, 1/0 ➔ power on/power off
* Bit 2,1 (CALL_2,CALL_1) : Bank selections for Caller ID RAM
  00 to 11 are four blocks of CALLER ID RAM area. User can use 1.0K RAM by RC register.
* Bit 3~4 = 0 : unused
* Bit 5 (SDTPW/0) : Power control of Stuttered dial tone circuit/disable SDT

ps. When code option bit2(/SDTEN) is "1", SDT is disabled and IOCA bit5 is always "0". User cannot use SDT function. When code option bit2(/SDTEN) is "0", SDT is enabled and IOCA bit5 is SDTPW. At this time, setting SDTPW 1/0 ➔ power on SDT circuit /power down SDT circuit.

* Bit 6~7 = 0 : unused

7. IOCB (Preset and readout for COUNTER1)

PAGE0 (unused)

It is unused and always "00000000".

PAGE1 (COUNTER1 preset and readout)

It is 8 bit up-counter (COUNTER1) preset and read out register. (write = preset) After an interruption, it will count from "00".

8. IOCC (Preset and readout for COUNTER2)

PAGE0 (unused)

It is unused and always "00000000".

PAGE1 (COUNTER2 preset and readout)

It is 8 bit up-counter (COUNTER2) preset and read out register. (write = preset) After an interruption, it will count from "00".

9. IOCD (Internal pull-high control for PORT7, R-option control for PORT9)

PAGE0 (Internal pull-high control for P77~P70 pins)

7	6	5	4	3	2	1	0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

* Bit 7~0 (PH7~PH0) : PORT7's internal pull-high control for P77~P70 pins, 1/0 ➔ enable/disable

PAGE1 (R-option control for P97~P90)

7	6	5	4	3	2	1	0
RO7	RO6	RO5	RO4	RO3	RO2	RO1	RO0

* Bit 7~0 (RO7~RO0) : R-option control bits for P97~P90 pins, 1/0 ➔ enable /disable

RO is used for R-option. Setting RO to '1' will enable the status of R-option pin (P90 ~ P97) to read by controller. Clearing RO will disable R-option function. If the R-option function is used, user must connect PORT9 pins to GND by 560K external register. If the register is connected/disconnected, the R9 will read as " 0/1" when RO is set to '1'.

10. IOCE (PORT7's P77 switch, COUNTER1 and COUNTER2 source, COUNTER1's prescaler, FSK output data type)

PAGE0 (PORT7's P77 switch)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LBD/P77	0

* Bit 0 = 0 : unused
* Bit 1 (LBD/P77) : PORT7's P77 switch, 0/1 ➔ low battery detect input/ normal IO port P77
* Bit 2~7 = 0 : unused

PAGE1 (P77's and P76's open-drain control, COUNTER1 and COUNTER2 source, COUNTER1's prescaler, FSK output data type)

7	6	5	4	3	2	1	0
OP77	OP76	C2S	C1S	PSC1	PSC0	CDRD	0

* Bit 0 = 0 : unused
* Bit 1 (CDRD) : FSK output data type selection bit, 0/1 ➔ FSK cooked data/FSK raw data
* Bit 3,2 (PSC1,PSC0) : COUNTER1's prescaler, reset = (0,0)
  (PSC1,PSC0) = (0,0) ➔ 1:1, (0,1) ➔ 1:4, (1,0)➔ 1:8, (1,1) ➔ reserved
* Bit 4 : COUNTER1 source, 0/1 ➔ 32.768KHz/3.579MHz if enable
* Bit 5 : COUNTER2 source, 0/1 ➔ 32.768KHz/3.579MHz if enable prescale=1:1
* Bit 6 : P76's open-drain control, 0/1 ➔ disable/enable
* Bit 7 : P77's open-drain control, 0/1 ➔ disable/enable

11. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
INT3	FSK/CW	C8_2	C8_1	INT2	INT1	INT0	TCIF

* Bit 0 ~ Bit 7 are interrupt enable bits, 0/1 ➔ disable/enable interrupt
IOCF Register is readable and writable.

VII.3 TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8-bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 10 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

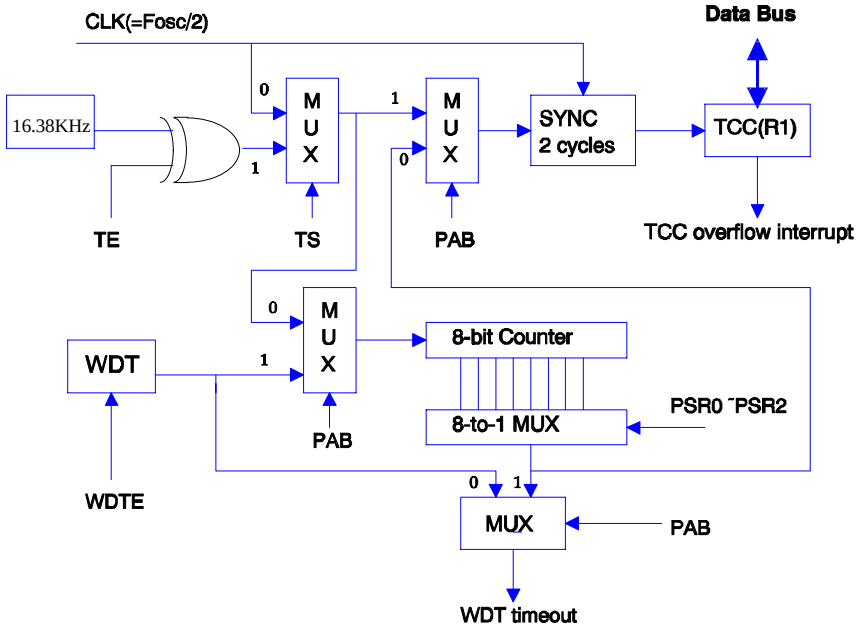


Fig.10 Block diagram of TCC WDT

VII.4 I/O Ports

The I/O registers, PORT5 ~ PORT7 and PORT9, are bi-directional tri-state I/O ports. PORT7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5 ~ IOC7 and IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.11.

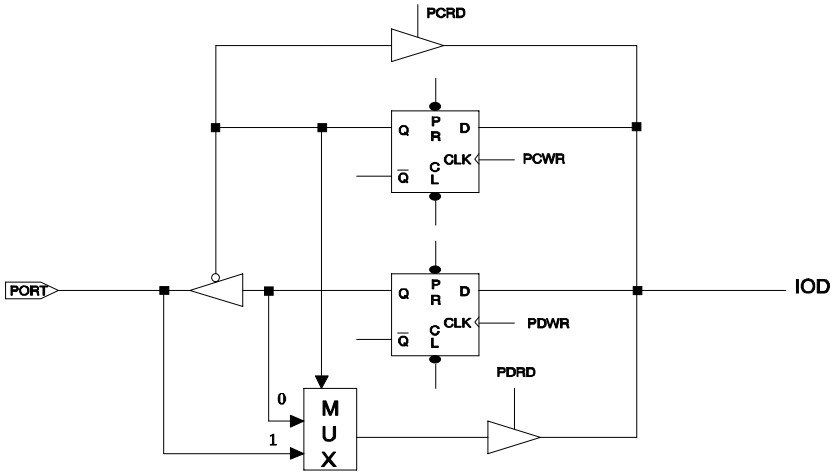


Fig.11 The circuit of I/O port and I/O control register

VII.5 RESET and Wake-up

The RESET can be caused by

(1) Power on reset, or Voltage detector

(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

Note that only Power on reset, or only Voltage detector in Case (1) is enabled in the system by CODE-Option bit.

If Voltage detector is disabled, Power on reset is selected in Case (1). Refer to Fig.12.

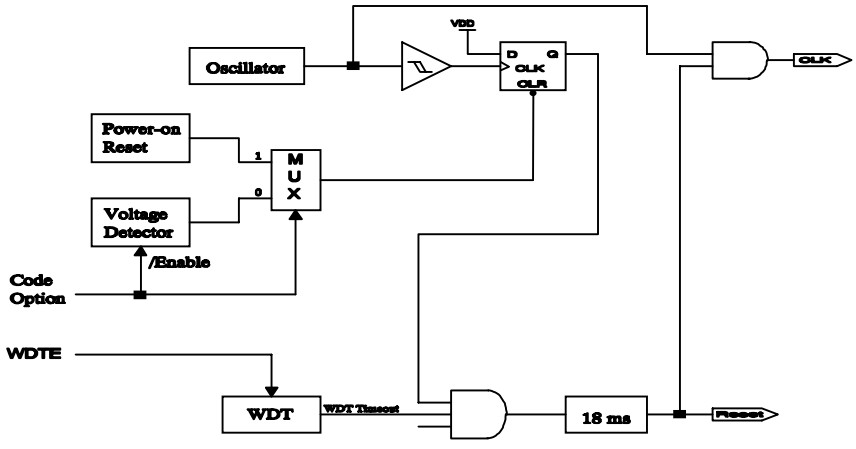


Fig.12 Block diagram of Reset of controller

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)

R5 = PORT"0000"	IOC5 = "1111xx00"	
R6 = PORT	IOC6 = "11111111"	
R7 = PORT	IOC7 = "11111111"	
R8 = "xxxxxxxx"	IOC8 = "00000000"	
R9 = PORT	IOC9 = "11111111"	
RA = "000x0xxx	IOCA = "00000000"	
RB = "11111111"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "00000000"	Page1 IOCC = "00000000"
RD = "xxxxxxxx"	Page0 IOCD = "00000000"	Page1 IOCD = “00000000”
RE = "00000000"	Page0 IOCE = "00000010"	Page1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	

The controller can be awakened from SLEEP mode or IDLE mode (execution of "SLEP" instruction, named as SLEEP mode or IDLE mode) by (1) TCC time out (IDLE mode only) (2) WDT time-out (if enabled) (3) external input at PORT9. The three cases will cause the controller to be wake-up and run from next instruction in IDLE mode, reset in SLEEP mode. After CPU is wake-up, user should control Watchdog in case of reset in GREEN mode or NORMAL mode. The last two should be open RE register before into SLEEP mode or IDLE mode. The first one case will set a flag in RF bit 0. But will go to address 0x08.

VII.6 Interrupt

The CALLER ID IC has internal interrupts which are falling edge triggered, as follows : TCC timer overflow interrupt (internal) , two 8-bit counters overflow interrupt .

If these interrupt sources change signal from high to low , then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0, INT1, INT2 and INT3. And four internal counters interrupt available.

Internal signals include TCC, CNT1, CNT2, FSK and CALL WAITING data. The last two will generate an interrupt when the data transient from high to low.

External interrupt INT0, INT1, INT2 and INT3 signals are from PORT7 bit0 to bit3 . If IOCF is enable then these signal will cause interrupt , or these signals will be treated as general input data .

After reset, the next instruction will be fetched from address 000H and the instruction interrupt is 001H and the hardware interrupt is 008H.

TCC will go to address 0x08 in GREEN mode or NORMAL mode after time out. And it will run next instruction from “SLEP” instruction and then go to address 0x08 in IDLE mode. These two cases will set a RF flag.

It is very important to save ACC, R3 and R5 when processing an interruption.

Address	Instruction	Note
0x08	DISI	;Disable interrupt
0x09	MOV A_BUFFER,A	;Save ACC
0x0A	SWAP A_BUFFER	
0x0B	SWAPA 0x03	;Save R3 status
0x0C	MOV R3_BUFFER,A	
0x0D	MOV A,0x05	;Save ROM page register
0x0E	MOV R5_BUFFER,A	
:	:	
:	:	
:	MOV A,R5_BUFFER	;Return R5

:	MOV 0X05,A	
:	SWAPA R3_BUFFER	;Return R3
:	MOV 0X03,A	
:	SWAPA A_BUFFER	;Return ACC
:	RETI	

VII.7 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z

0	0100	11rr	rrrr	04rr	COM R	/R → R	Z
0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1	1110	1000	kkkk	1E8k	PAGE k	K->R5(3:0)	None
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

VII.8 CODE Option Register

The CALLER ID IC has one CODE option register that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7	6	5	4	3	2	1	0
-	-	-	/RTFEN	/MEIEN	/SDTEN	/POVD	MCLK

* Bit 0 (MCLK) : Main clock selection, 0/1 ➔ 3.58MHz /1.79MHz
* Bit 1 (/POVD) : Power on voltage detector control, 0/1 ➔ enable/disable

/POVD	2.2V POVD reset	1.8V power on reset	sleep mode current
1	No	Yes	1uA typical
0	Yes	Yes	15uA typical

* Bit 2 (/SDTEN) : Stuttered dial tone function control, 0/1 ➔ enable/disable
* Bit 3 (/MEIEN) : MEI function control, 0/1 ➔ enable/disable MEI function
  When MEI function is disabled, MEI is always powered down and user cannot use this function.

* Bit 4 (/RTFEN) : RTF function control, 0/1 ➔ enable/disable RTF function
  When RTF function is disabled, RTF is always powered down and user cannot use this function.
* Bits 5~7 : unused, must be "0"s.

VII.9 FSK FUNCTION

VII.9.1 Functional Block Diagram

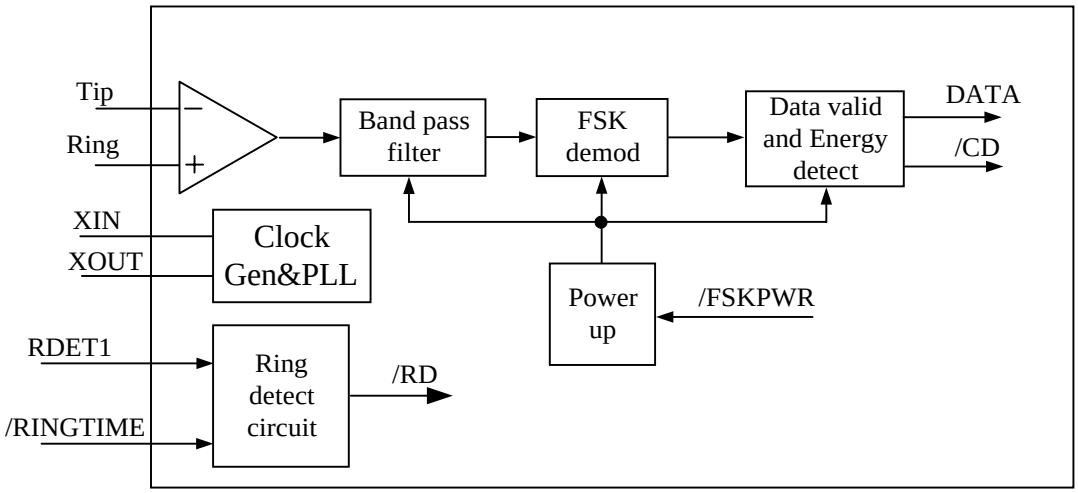


Fig.13 FSK Block Diagram

VII.9.2 Function Descriptions

The CALLER ID IC is a CMOS device designed to support the Caller Number Deliver feature which is offered by the Regional Bell Operating Companies.The FSK block comprises two paths: the signal path and the ring indicator path. The signal path consists of an input differential buffer, a band pass filter, an FSK demodulator and a data valid with carrier detect circuit. The ring detector path includes a clock generator, a ring detect circuit.

In a typical application, the ring detector maintains the line continuously while all other functions of the chip are inhibited. If a ring signal is sent, the /RINGTIME pin will has a low signal. User can use this signal to wake up whole chip or read /RD signal from RA register.

A /FSKPWR input is provided to activate the block regardless of the presence of a power ring signal. If /FSKPWR is sent low, the FSK block will power down whenever it detects a valid ring signal, it will power on when /FSKPWR is high.

The input buffer accepts a differential AC coupled input signal through the TIP and RING input and feeds this signal to a band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post filter. The output data is then made available at DATA OUT pin. This data, as sent by the central office, includes the header information (alternate "1" and "0") and 150 ms of marking which precedes the date, time and calling number. If no data is present, the DATA OUT pin is held in a high state. This is accomplished by a carrier detect circuit which determines if the in-band energy is high enough. If the incoming signal is valid and thus the demodulated data is transferred to DATA OUT pin. If it is not, then the FSK demodulator is blocked.

VII.9.3 Ring detect circuit

When Vdd is applied to the circuit, the RC network will charge cap C1 to Vdd holding /RING TIME off. The resistor network R2 to R3 attenuates the incoming power ring applied to the top of R2. The values given have been chosen to provide a sufficient voltage at DET1 pin, to turn on the Schmitt trigger input. When Vt+ of the Schmitt is exceeded, cap C1 will discharge.

The value of R1 and C1 must be chosen to hold the /RING TIME pin voltage below the Vt+ of the Schmitt between the individual cycle of the power ring. With /RINGTIME enabled, this signal will be a /RD signal in RA through a buffer.

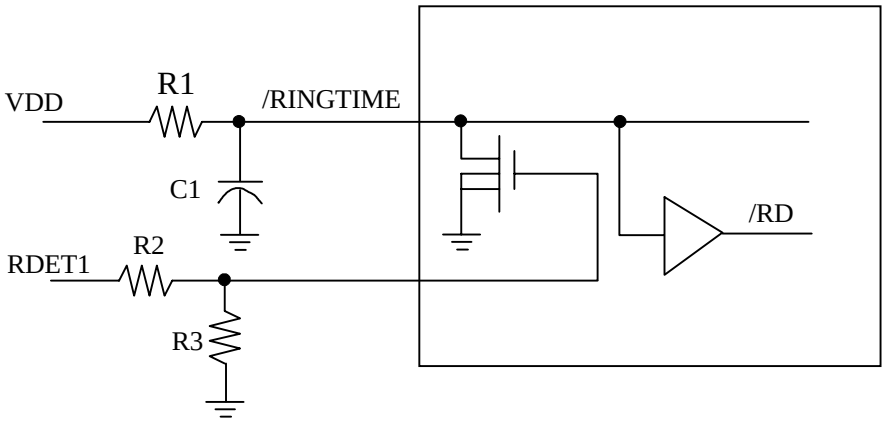


Fig.14 ring detect circuit

VII.10 DTMF (Dual Tone Multi Frequency) Tone Generator

Built-in DTMF generator can generate dialing tone signals for telephone of dialing tone type. There are two kinds of DTMF tone. One is the group of row frequency, the other is the group of column frequency, each group has 4 kinds of frequency, and user can get 16 kinds of DTMF frequency totally. DTMF generator contains a row frequency sine wave generator for generating the DTMF signal, which selected by low order 4 bits of RB and a column frequency sine wave generator for generating the DTMF signal, which selected by high order 4 bits of RB. This block can generate single tone by filling one bit zero to this register.

If all the values are high, the power of DTMF will turn off until one or two low values.

Either high or low 4 bits must be set by an effective value, otherwise, if any ineffective value or both 4 bits are load effective value, tone output will be disable. Recommend value refer to table as follow please :

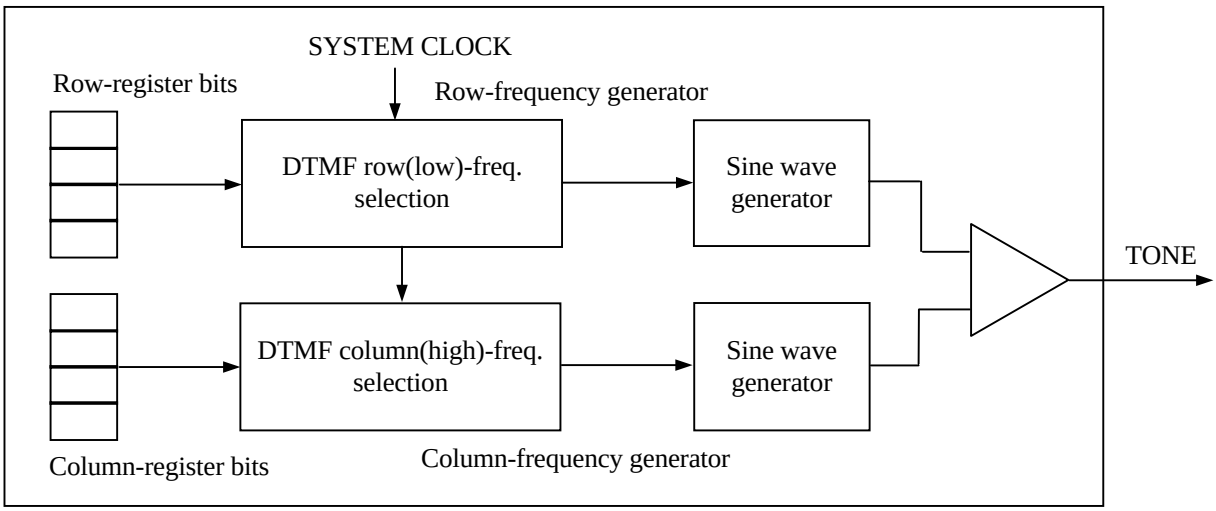


Fig.15 DTMF Block Diagram

* RB (DTMF Register)
. Bit 0 - Bit 3 are row-frequency tones.
. Bit 4 - Bit 7 are column-frequency tones.
. Initial RB is equal to HIGH.
. Except below values of RB, the other values of RB are not effect. If RB is set by ineffective value, the DTMF output will be disable and there is no tone output.
. Bit 7 ~ 0 are all "1" turn off DTMF power.

	Bit 7~4 (column freq.)			
Bit 3~0 (row freq.)	1110 (1203.0Hz)	1101 (1331.8Hz)	1011 (1472Hz)	0111 (1645.2Hz)
1110 (699.2Hz)	1	2	3	A
1101 (771.6Hz)	4	5	6	B
1011 (854.0Hz)	7	8	9	C
0111 (940.1Hz)	*	0	#	D

VII.11 CALL WAITING Function Description

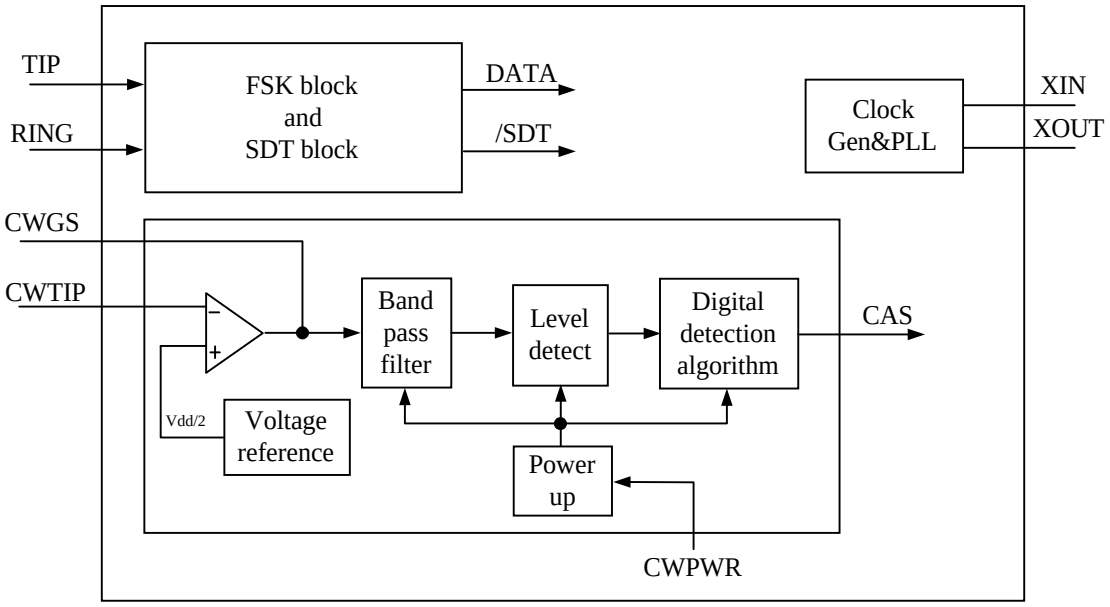


Fig.16 Call Waiting Block Diagram

Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. This way the customer can still receive important calls while engaged in a current call. The CALL WAITING DECODER can detect CAS (Call-Waiting Alerting Signal 2130Hz plus 2750Hz) and generate a valid signal on the data pins.

The call waiting decoder is designed to support the Caller Number Deliver feature, which is offered by regional Bell Operating Companies. The call waiting decoder has four blocks, including pre-amplifier, band pass filter, level detect and digital detection algorithm.

In a typical application, after enabling CW circuit (by RE BIT7 CWPWR) this IC receives Tip and Ring signals from twisted pairs. The signals as inputs of pre-amplifier, and the amplifier sends input signal to a band pass filter. Once the signal is filtered, the digital detection block decodes the information and sends it to R3 register bit7. The output data made available at R3 CAS bit.

The data is CAS signals. The CAS is normal high. When this IC detects 2130Hz and 2750Hz frequency, then CAS pin goes to low.

VII.12 Stuttered dial tone (SDT) Function Description

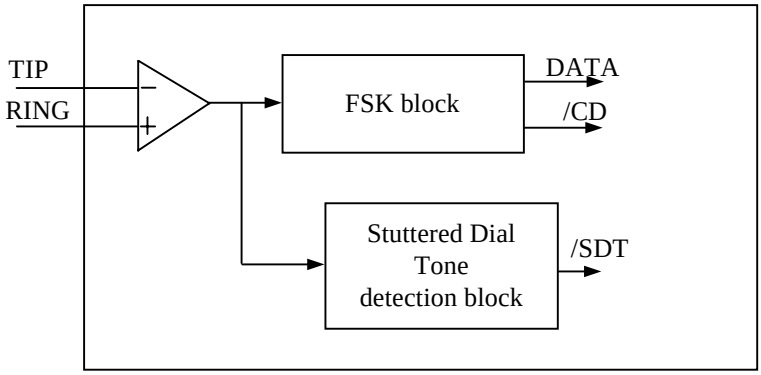


Fig.17 Stuttered dial tone block diagram

SDT (Stuttered dial tone) circuit and FSK circuit use the same input OP Amp. **When SDTPW bit (IOCA bit5) is set, SDT circuit is powered on and SDT detection is enabled. SDT detection enabled means it is powered on and detects 350Hz plus 440Hz dual tone frequency**. And SDT signal detection output is sent to /SDT bit (R3 bit5) with low enable. If SDT circuit works, it consists of high-band and low-band band pass tone filters, level detect, frequency counting and digital algorithm to qualify correct timing.

VII.13 MEI and RTF Function Description

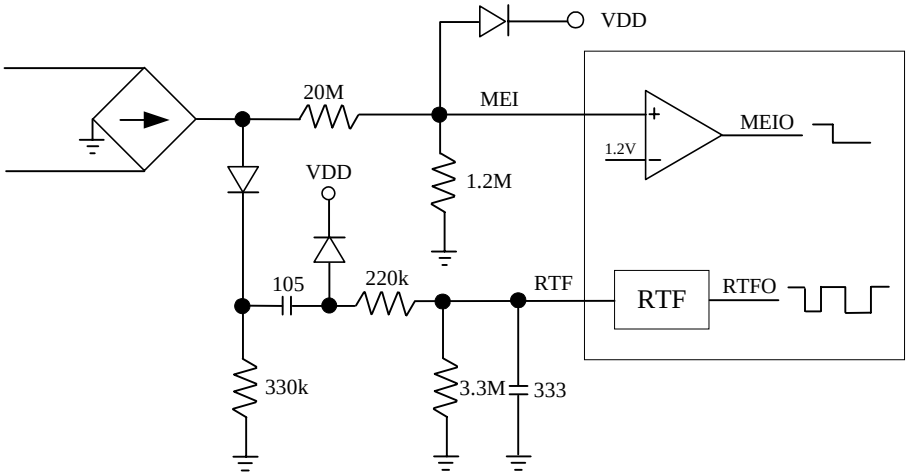


Fig.18 MEI & RTF

Based on TIA/EIA-777 (or TIA SP-4078) protocol, MEI (Multiple Extension Internetworking) allows Type 2 (and 3) CPE to dynamically arbitrate responsibility for completing the CAS-ACK handshake. Also, RTF (Request to Flash) allows Type 2 (and 3) CPE to synchronize line flash signal after CAS-ACK handshaking.

For MEI part, protocol shows line voltage below 19V as line-in use (phone off-hook status) and voltage above 21V as line high (phone on-hook status). MEI circuits works as on-hook/off-hook detection and internal transition voltage is 1.2V. Use two external resistors to reduce line DC voltage into MEI input pin. These has a little voltage transition hysteresis to complete the rule.

For RTF part, protocol shows 0.5V line DC voltage change detection and timing to be followed (see the protocol for details). RTF circuit can detect this little DC voltage change and complete the same timing as protocol shown.

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	Vdd	-0.3 To 6	V
INPUT VOLTAGE	Vin	-0.5 TO Vdd +0.5	V
OPERATING TEMPERATURE RANGE	Ta	0 TO 70	℃

IX. DC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=5.0V±5%, VSS=0V)
(VDD=2.5V to 6V for CPU, DTMF ; VDD=3.5V to 6V for FSK, VDD=3.0V to 6V for CW, SDT)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input Leakage Current for bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input High Voltage	VIH		2.5			V
Input Low Voltage	VIL				0.8	V
Input High Threshold Voltage	VIHT	/RESET, TCC, RDET1	2.0			V
Input Low Threshold Voltage	VILT	/RESET, TCC,RDET1			0.8	V
Clock Input High Voltage	VIHX	OSCI	3.5			V
Clock Input Low Voltage	VILX	OSCI			1.5	V
Key scan Input High Voltage	VHscan	Port6 for key scan	3.5			V
Key scan Input Low Voltage	VLscan	Port6 for key scan			1.5	V
Output High Voltage (port5,6,7)	VOH1	IOH = -1.6mA	2.4			V
(port9)		IOH = -6.0mA	2.4			V
Output Low Voltage (port5,6,7)	VOL1	IOL = 1.6mA			0.4	V
(port9)		IOL = 6.0mA			0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS		-10	-15	μA
Power down current (SLEEP mode) POVD disable	ISB1	All input and I/O pin at VDD, output pin floating, WDT disabled		1	4	μA
Power down current (SLEEP mode) POVD enable				12	20	uA
Low clock current (GREEN mode) POVD disable	ISB2	CLK=32.768KHz, FSK, DTMF, CW, SDT block disable , All input and I/O pin at VDD, output pin floating, WDT disabled		65	80	μA
Low clock current (GREEN mode) POVD enable				75	95	uA
Low clock current (IDLE mode) POVD disable	ISB3	CLK=32.768KHz, FSK, DTMF, CW, SDT block disable , All input and I/O pin at VDD, output pin floating, WDT disabled,CPU disable		45	60	μA
Low clock current (IDLE mode) POVD enable				55	75	uA
Operating supply current	ICC1	/RESET=High,		1.5	1.8	mA

(CPU enable)		CLK=3.579MHz, output pin floating, FSK, DTMF, CW, SDT block disable				
Tone1 signal strength	**V1rms**	**Root mean square voltage**	**130**	**155**	**180**	**mV**
Tone2 signal strength	**V2rms**	**Root mean square voltage**	**1.259V1rms**			**mV**

Ps. V1rms and V2rms has 2 dB difference. It means 20log(V2rms/V1rms) = 20log1.259 = 2 (dB)

IX. AC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=5.0V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.579MHz		60 550		us ns
Device delay hold time	Tdrh			18		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		18		ms

Note 1: N= selected prescaler ratio.

(FSK Band Pass Filter AC Characteristic)(Vdd=+5.0V,Ta=+25℃)

CHARACTERISTIC	Min	Typ	Max	Unit
input sensitivity TIP and RING pin1 and pin2 Vdd=+5V	-40	-48	--	dBm

(Call waiting Band Pass Filter AC Characteristic) (V_{DD}=+5.0V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
input sensitivity TIP and RING pins ,Vdd=+5V, Input G=1		-38		dBm

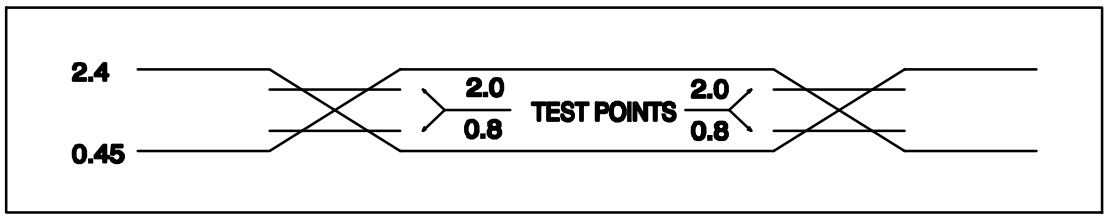
(Stuttered dial tone AC Characteristic) (VDD=+5.0V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
input sensitivity TIP and RING pins ,Vdd=+5V		-38		dBm
Input frequency tolerance		± 2.0		%

Description	Symbol	Min	Typ	Max	Unit
(FSK AC Characteristics)					
OSC start up(32.768KHz) (3.579MHz PLL)	Tosc	--	300	400 10	ms
(FSK AC Characteristic)					
Carrier detect low	Tcdl	--	10	14	ms
Data out to Carrier det low	Tdoc	--	10	20	ns
Power up to FSK(setup time)	Tsup	--	15	20	ms
/RD low to /RINGTIME low	Trd			50	ms
End of FSK to Carrier Detect high	Tcdh	8	--	--	ms
(Call waiting AC Characteristics)					
CAS input signal length (2130 ,2750 Hz @ -20dBm)	Tcasi		80		ms
Data detect delay time	Td		42		ms
Data release time	Tr		26		ms
(Stuttered dial tone AC characteristics)					
Stuttered dial tone signal detect delay time	Tstdd		30		ms
Stuttered dial tone signal release time	Tstdr		30		ms

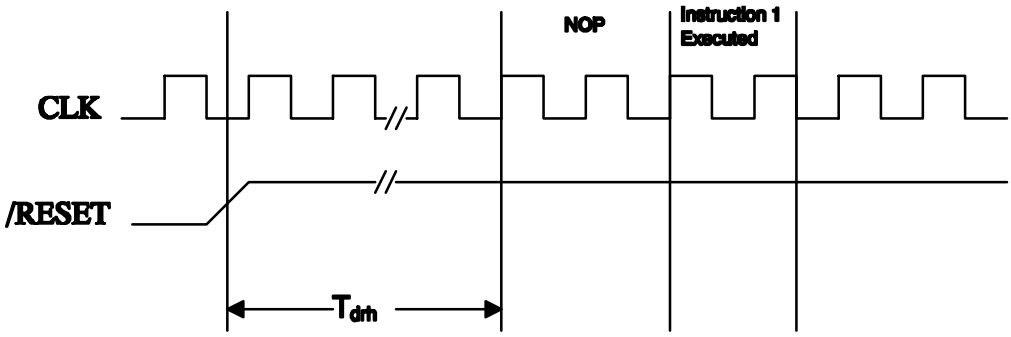
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

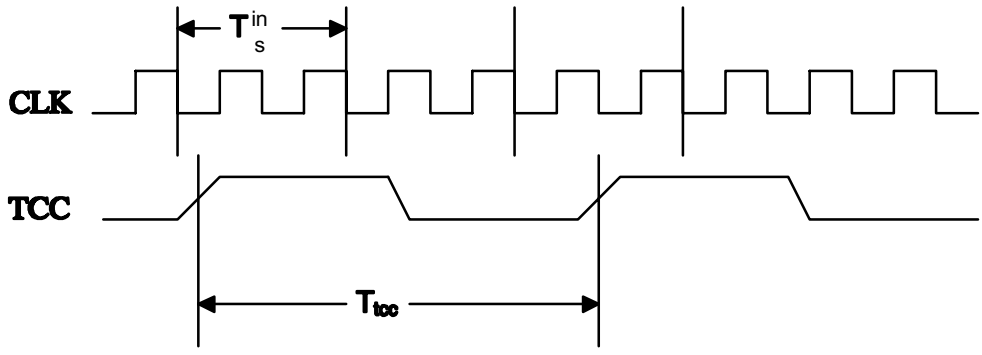


Fig.19 AC timing

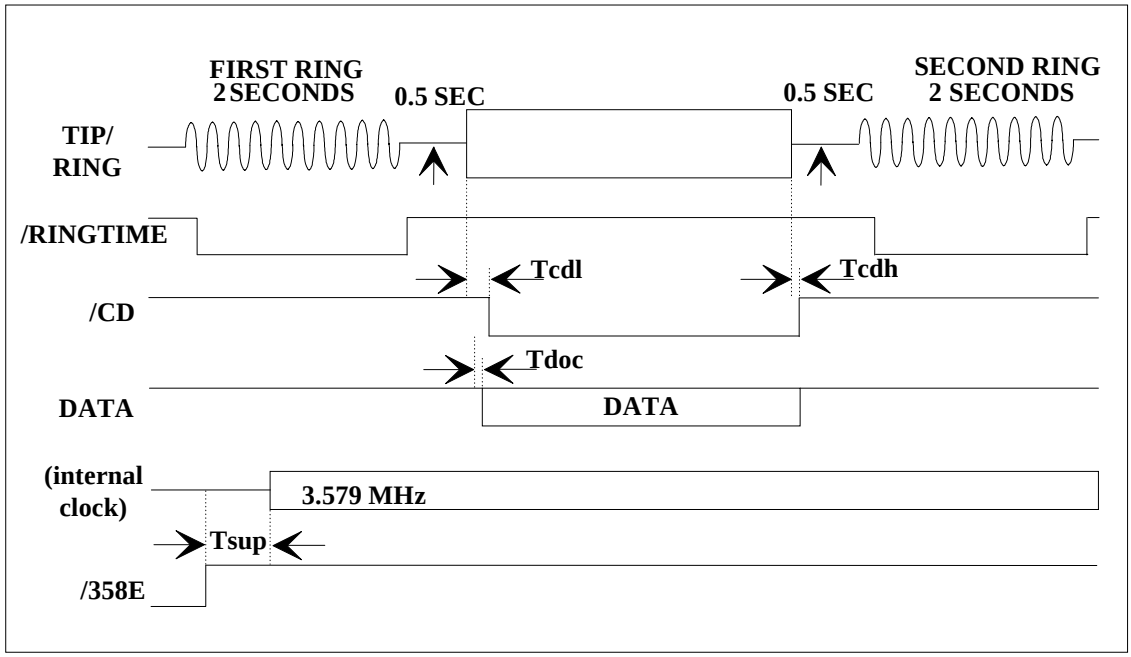


Fig.20 FSK Timing Diagram

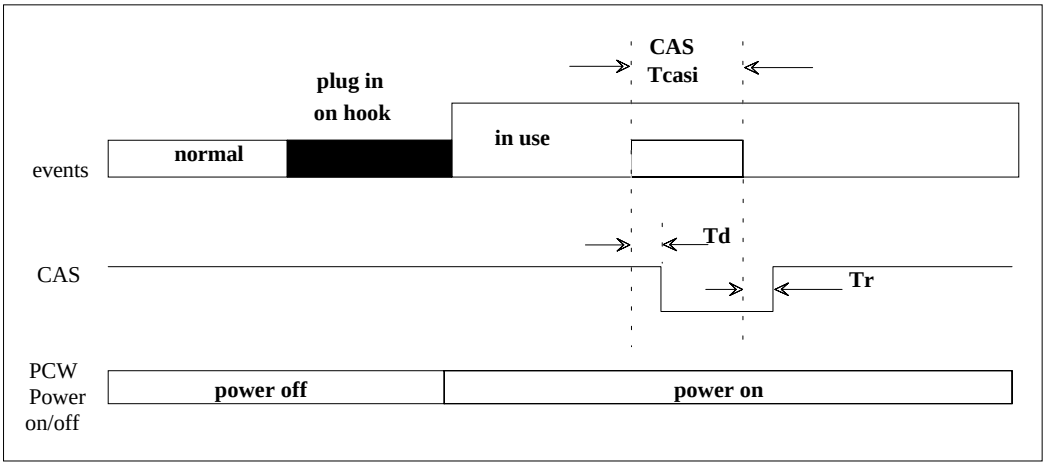


Fig.21 Call Waiting Timing Diagram

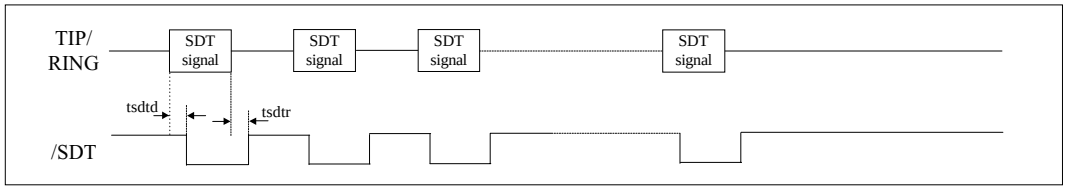


Fig.22 Stuttered dial tone detect. timing diagram

XII. Application Circuit

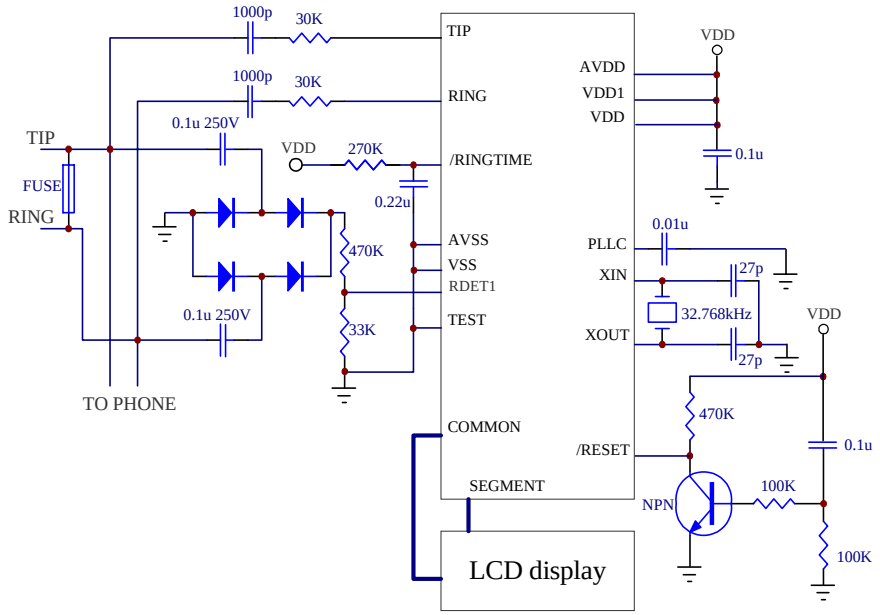


Fig.23a APPLICATION CIRCUIT for **EM78910**

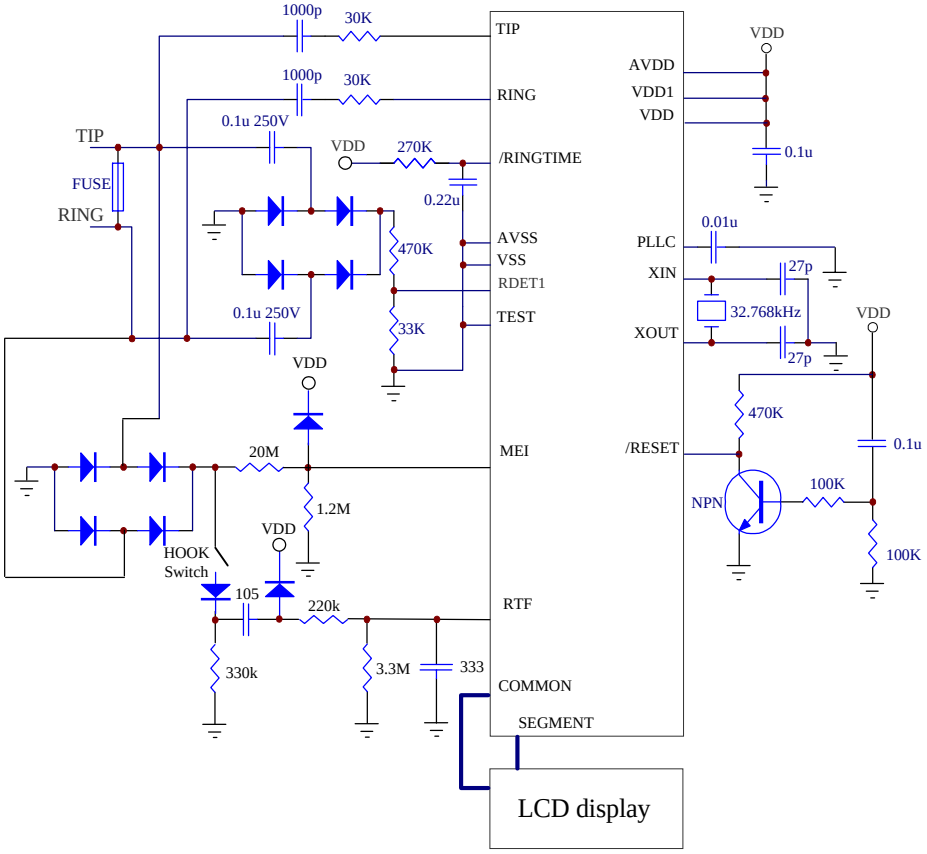


Fig.23b APPLICATION CIRCUIT for **EM78910A**